

SIGMA-DELTA MODULATOR WITH PASSIVE BANDPASS LOOP FILTER

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to the field of  
5 signal processing and more specifically to a sigma-delta  
modulator with passive bandpass.

BACKGROUND OF THE INVENTION

Bandpass sigma-delta modulation typically involves using active filters to perform filtering functions in the feedback loop. Active filters, however, may include 5 active components such as operational amplifiers and LC circuits that may consume a significant amount of power. Additionally, depending on the active components in the active filters may require the sigma-delta modulation to run at limited resolution. Consequently, known sigma-10 delta modulation may be unsatisfactory in certain situations.

SUMMARY OF THE INVENTION

In accordance with the present invention, disadvantages and problems associated with previous techniques of bandpass sigma-delta modulation may be reduced or eliminated.

According to one embodiment, digitizing a signal includes sampling and holding an analog signal to yield a sampled signal, where the analog signal includes information. The sampled signal is filtered at a passive filter circuit to yield a filtered signal. The passive filter circuit includes at least one passive element and the filtered signal is characterized by a bandpass response. The filtered signal is quantized to yield a digital signal, where the digital signal corresponds to the analog signal and the digital signal includes the information.

Certain embodiments of the invention may provide one or more technical advantages. A technical advantage of one embodiment may be that a bandpass sigma-delta modulator does not require the use of active components in the loop filter, which may allow the modulator to run at low power and low voltage. Another technical advantage of one embodiment may be that the bandpass sigma-delta modulator may operate at a high sampling rate, which may allow the bandpass sigma-delta modulator to yield a higher resolution while maintaining low power consumption.

Certain embodiments of the invention may include none, some, or all of the above technical advantages. One or more other technical advantages may be readily apparent to one skilled in the art from the figures, descriptions, and claims included herein.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and its features and advantages, reference is now made to the following description, taken in conjunction with the accompanying drawings, in which:

FIGURE 1 is a block diagram of an embodiment of a bandpass sigma-delta modulator that may be used in accordance with the present invention;

FIGURE 2 is an example of a timing diagram that may be used with the bandpass sigma-delta modulator of FIGURE 1;

FIGURE 3 is a circuit diagram of an embodiment of the bandpass sigma-delta modulator of FIGURE 1 that may be used in accordance with the present invention; and

FIGURE 4 is an example of a timing diagram that may be used with the bandpass sigma-delta modulator of FIGURE 3.

DETAILED DESCRIPTION OF THE DRAWINGS

Embodiments of the present invention and its advantages are best understood by referring to FIGURES 1 and 2 of the drawings, like numerals being used for like and corresponding parts of the various drawings.

FIGURE 1 is a block diagram of an embodiment of a bandpass sigma-delta modulator 10. In general, bandpass sigma-delta modulator (SDM) 10 converts an analog signal 20 into a digital signal 22 by filtering a sampled analog signal using a passive bandpass loop filter 18. A quantizer 16 converts the filtered signal to digital signal 22. According to the illustrated embodiment, bandpass SDM 10 includes a sample-hold circuit 12, a passive bandpass loop filter 18, and a quantizer 16 coupled as shown in FIGURE 1.

Sample-hold circuit 12 receives a control signal to sample and hold analog signal 20. According to one embodiment, sample-hold circuit 12 samples and holds analog signal 20 in response to a pulse of control signal  $\varphi_{2m}$ . Sample-hold circuit 12 also receives a feedback signal comprising digital signal 22, and sums the analog signal 20 and digital signal 22. According to the illustrated embodiment, sample-hold circuit 12 comprises a high-speed sample-hold circuit that is shared among the multiple filter paths 13 of passive bandpass loop filter 18. Sample-hold circuit 12 may also convert mismatch errors between the signals of the filter paths into an overall gain or phase error. By sharing sample-hold circuit 12 between the filter paths, more efficient matching of gain and phase between the signals of the filter paths may be accomplished at a high speed sampling rate.

Passive bandpass loop filter 18 receives the sampled signal and one or more control signals to filter the sampled signal. For example, passive bandpass loop filter 18 filters the sampled signal to yield a filtered signal according to a bandpass response. According to one embodiment, passive bandpass loop filter 18 comprises  $N$  filter paths 13 placed in parallel to perform the bandpass response. According to the illustrated embodiment, a passive highpass filters 14 may be used at each filter path 13 in order to generate the filtered signal according to a bandpass response. Using highpass filters 14 instead of low pass filters may result in more efficient hardware. Any other suitable passive filter circuit may be used at each filter path without departing from the scope of the invention.

According to the illustrated embodiment, passive bandpass loop filter 18 comprises switches  $S_{jk}$ , where  $j=1,\dots,n$  and represents a switch of a filter path  $k$ , and where  $k=1,\dots,N$  and represents the filter path at which the switch is located. For example, switch  $S_{11}$  represents the first switch of the first filter path. Switches  $S_{jk}$  are activated according to pulses of a corresponding control signal 24. For example, switch  $S_{11}$  may be activated according to a pulse of a corresponding control signal  $\varphi_{11}$ . Examples of control signals are described with reference to FIGURE 2. Passive bandpass loop filter 18 may include any number of switches  $S_{jk}$  without departing from the scope of the invention.

Passive bandpass loop filter 18 includes a passive switched capacitor (SC) highpass filter 14 at each filter path 13. Although in this embodiment a highpass filter has been described, it will be understood that any other

suitable filter response such as a low pass filter may be used. According to the illustrated embodiment, passive SC highpass filter 14 operates according to a transfer function  $H$  as described by Equation (1):

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$$H = \frac{\alpha}{1 + (1 - \alpha) z^{-k}} \quad (1)$$

where  $\alpha$  is the RC coefficient corresponding to the passive filter components,  $k$  represents the filter path, and  $z^{-1}$  represents one clock cycle delay. Placing passive SC highpass filters 14 in parallel may result in a transfer function  $Y$  as described by Equation (2):

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$$Y = \frac{\alpha}{1 + (1 - \alpha) z^{-N}} \quad (2)$$

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where transfer function  $Y$  has a passband centered at approximately  $F_s(i/2N)$  with  $F_s$  representing the sampling frequency at which bandpass sigma-delta modulator 10 operates.

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Quantizer 16 quantizes the filtered signal from each passive bandpass loop filter 18. According to the illustrated embodiment, quantizer 16 comprises a one bit high speed comparator that quantizes the filtered signals to generate a digital signal 22. Quantizer 16 may be activated according to a main control signal  $\bar{\Phi}_{2m}$  in order for quantizer 16 to generate a bit at substantially every low pulse of main control signal  $\bar{\Phi}_{2m}$ . Quantizer 16 may also direct digital signal 22 to sample-hold circuit 12 to form a feedback loop that feeds digital signal 22 to be summed with the sampled analog signal at sample-hold

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circuit 12. The feedback loop may include additional filters, circuits, components, converters, and processors without departing from the scope of the invention.

Modifications, additions, or omissions may be made 5 to bandpass SDM 10 without departing from the scope of the invention. For example, passive SC highpass filter 14 may be configured using any other suitable filter such as a lowpass filter without departing from the scope of the invention. As another example, passive bandpass loop 10 filter 18 may include any suitable number of passive SC highpass filters 14. Additionally, functions may be performed using any suitable logic comprising software, hardware, other logic, or any suitable combination of the preceding. "Each" as used in this document refers to 15 each member of a set or each member of a subset of a set.

FIGURE 2 is an example of a timing diagram illustrating control signals that may be used with the bandpass SDM 10 of FIGURE 1. FIGURE 3 is a circuit diagram of an embodiment of the bandpass sigma-delta 20 modulator 10 of FIGURE 1. FIGURE 4 is an example of a timing diagram illustrating control signals that may be used with bandpass SDM 10 of FIGURE 3.

FIGURE 2 is an example of a timing diagram 24 illustrating control signals that may be used with the 25 bandpass SDM 10 of FIGURE 1. For example, timing diagram 24 includes control signals  $\varphi_{2m}$ ,  $\varphi_{11}$ ,  $\varphi_{1N}$ ,  $\varphi_{21}$ , and  $\varphi_{2N}$ . Any other number of signals may be used without departing from the scope of the invention. For example, for bandpass SDM 10 having more than two filter paths 13, 30 timing diagram 24 may include additional control signals.

FIGURE 3 is a circuit diagram of an embodiment of the bandpass sigma-delta modulator 10 of FIGURE 1.

According to the illustrated embodiment, bandpass SDM 10 is configured as a two-path fourth-order passive bandpass sigma-delta modulator. Passive bandpass loop filter 18 comprises a first passive SC highpass filter 14a and a second passive SC highpass filter 14b. As illustrated, first and second passive SC highpass filter 14a and 14b comprise fourth-order passive filters. Passive bandpass loop filter 18 may comprise any suitable number of passive SC highpass filters 14. Passive SC highpass filters 14 may comprise a higher or lower order of passive filter without departing from the scope of the invention.

Sample-hold circuit 12 comprises sampling capacitors  $C_{R1}$  that are shared between the passive SC highpass filters 14a-b. According to one embodiment, sampling capacitors  $C_{R1}$  are switched at a sampling frequency  $F_s$ . At a sampling frequency  $F_s$  and with two filter paths of bandpass SDM 10, input analog signal 20 may comprise any Intermediate Frequency (IF) signal having a maximum frequency of  $F_s(i/4)$ .

According to the illustrated embodiment, pulses of second control signal  $\varphi_2$  having a sampling frequency  $F_s$  activate switches at sample-hold circuit 12 that sample and hold the input voltage IF signals  $V_{IFP}$  and  $V_{IFM}$ . According to the illustrated embodiment, during a pulse of first control signal  $\varphi_1$ , sampling capacitors  $C_{R1}$  are charged to reference voltages  $V_{refp}$  and  $V_{refm}$ , and during a pulse of second control signal  $\varphi_2$ , input analog signal 20 is sampled and mixed with the appropriate reference voltage  $V_{refp}$  or  $V_{refm}$  to yield an analog sampled signal.

According to the illustrated embodiment, each passive SC highpass filter 14a-b comprises a switched

capacitor loop 32a-b and a fourth-order filtering loop 34a-b. For example, passive SC highpass filter 14a comprises switched capacitor loop 32a and fourth-order filtering loop 32b. Each switched capacitor loop 32a-b is controlled by first control signal  $\varphi_1$ , while each fourth-order filtering loop 34a-b is controlled by second control signal  $\varphi_2$ .

Passive SC highpass filters 14a-b filter the analog sampled signal using switched capacitor loops 32a-b, fourth-order filtering loops 34a-b, and clock signals  $I$  and  $Q$ . According to the illustrated embodiment, switched capacitor loop 32a-b and fourth-order filtering loop 34a-b filter the analog sampled signal according to a highpass response. Clock signals  $I$  and  $Q$  may be interleaved with the highpass response signal to yield a bandpass response. Clock signals  $I$  and  $Q$  may comprise odd-indexed clock signals  $\varphi_{I0}$  and  $\varphi_{Q0}$  and even-indexed clock signals  $\varphi_{IE}$  and  $\varphi_{QE}$ . Examples of clock signals are described in more detail with reference to FIGURE 4. Passive SC highpass filters 14 may include additional clock signals and additional control signals without departing from the scope of the invention. Additionally, switched capacitor loop 32a-b and fourth-order filtering loop 34a-b may filter the analog sampled signal according to any other suitable response, for example, a low pass response.

Quantizer 16 may comprise a one-bit quantizer that converts the bandpass response signal into a digital signal 22. According to the illustrated embodiment, quantizer 16 may be activated during the low pulses of second control signal  $\varphi_2$ . A feedback digital-to-analog (DAC) converter may be realized at node 28 at which the

bandpass response signal is fed to sample-hold circuit 12 via switched capacitors  $C_{R1}$ .

FIGURE 4 is an example of a timing diagram 26 illustrating control signals that may be used with bandpass SDM 10 of FIGURE 3. Timing diagram 26 illustrates clock signals  $I$  and  $Q$  and the timing of the pulses of the first and second control signals  $\varphi_1$  and  $\varphi_2$ . According to the illustrated example, control signals  $\varphi_1$  and  $\varphi_2$  are interleaved with clock signals  $\varphi_{I0}$ ,  $\varphi_{IE}$ ,  $\varphi_{Q0}$ , and  $\varphi_{QE}$ .

Modifications, additions, or omissions may be made to bandpass SDM 10 without departing from the scope of the invention. For example, the circuit that receives analog input 20 may be modified to include a mixing stage 30 as shown. Mixing stage 30 may comprise a Radio Frequency (RF) mixer or a transconductance circuit in order to supply a current-mode IF signal to the modulator instead of a voltage mode input signal. As another example, any suitable clock rate such as 104 MHz with an IF signal frequency of 26 MHz may be used to interleave signals at bandpass sigma-delta modulator 10. Additionally, functions may be performed using any suitable logic comprising software, hardware, other logic, or any suitable combination of the preceding.

Certain embodiments of the invention may provide one or more technical advantages. A technical advantage of one embodiment may be that a bandpass sigma-delta modulator does not require the use of active components in the loop filter, which may allow the modulator to run at low power and low voltage. Another technical advantage of one embodiment may be that the bandpass sigma-delta modulator may be operate at a high sampling

rate, which may allow the bandpass sigma-delta modulator to yield a higher resolution while maintaining low power consumption.

5       Although an embodiment of the invention and its advantages are described in detail, a person skilled in the art could make various alterations, additions, and omissions without departing from the spirit and scope of the present invention as defined by the appended claims.